2/4 B.Tech - FIRST SEMESTER

IT3L3 **DIGITAL SYSTEM DESIGN LAB** **Credits: 2**

Internal assessment: 25 marks

Lab: 3 Periods/week **Semester end examination: 50 marks**

Objectives:

- To verify basic logic gates.
- To verify half-adder and full-adder and its truth tables.
- To implement and verify Encoder\Decoder and Multiplexer\De-Multiplexer using logic gates.
- To verify state tables of RS, JK, T and D flip-flops using NAND & NOR gates.
- To verify Basic Shift Registers.

Outcomes:

Students will be able to

- Get practical knowledge on number systems.
- Get familiar with half-adder and full-adder logic circuits.
- Get familiar with Decoder, Encoder, Multiplexer and De-multiplexer circuits.
- Get familiar with Flip-Flops and its circuitry.
- Get familiar with basic shift registers and its circuitry.

Exercise 1

Boolean algebra: Theorems and logical guides, verification of truth tables

Exercise 2

Realization of Boolean expressions; Using (i) AND – OR-NOT Gates (ii) NAND Gates (iii) NOR Gates

Exercise 3

Code Converters: Binary – to- Gray, Gray- to -Binary

Exercise 4

Simplification of Boolean Functions

Exercise 5

Adders / Sub tractors: Half Adder, Full Adder,

Exercise 6

Multiplexers/ Data Selector: 2- input and 8- input, De-multiplexers, Logic Function Generator

Exercise 7

Decoders and Encoders.

Exercise 8

Comparators

Exercise 9

Latches Flip – Flops: RS, JK, T, D Flip – Flops.

Exercise 10
Counters: Binary Counter, Ripple Counter, Up/Down Counter

Exercise 11
Registers: Basic Shift Register (SR), SI/SO SR, SI/PO SR, PI/SO SR, PI/PO SR.

Exercise 12
Parity Generators/Checkers.

Reference Book:
1. Digital Design by M. Morris Mano, Michael D.Ciletti Pearson 4th Edition.